

Appl. No. 10/673,310
Examiner: EVERHART, CARIDAD, Art Unit 2891
In response to the Office Action dated June 9, 2005

Date: September 9, 2005
Attorney Docket No. 10112951

REMARKS

Responsive to the Office Action mailed on June 9, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103 as being unpatentable over Wang (US 2004/0153275) in view of Lee (US 5,977,558). Claim 4 is rejected under 35 U.S.C. 103 as being unpatentable over Wang in view of Lee and in further view of Jarvis (US 6,429,452). Claims 6-8 are withdrawn from consideration.

In this paper, claim 1 is amended to further clarify that each of the first and second memory cell structures has a deep trench capacitor and a vertical transistor structure formed in a substrate. Support for this amendment can be found in the original claim itself and on page 4, lines 12-20 and Fig. 1 of the application. Claims 3 and 6-8 are cancelled. Thus, after entry of this amendment, claims 1-2 and 4-5 remain in the application.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Rejections Under 35 U.S.C. 103(a)

Claims 1, 2 and 5 are rejected under 35 U.S.C. 103 as being unpatentable over Wang in view of Lee. Claim 4 is rejected under 35 U.S.C. 103 as being unpatentable over Wang in view of Lee and in further view of Jarvis. The rejections are respectfully traversed for at least the reasons as follow.

The invention of claim 1 is directed to a test device for detecting alignment of active areas and memory cell structures *in DRAM devices with vertical transistors*. The test device is

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disposed in a scribe line region of a wafer, and comprises parallel first and second memory cell structures disposed in the scribe line region, each having a deep trench capacitor and a vertical transistor structure formed in a substrate.

Whether taken alone or in combination, Wang, Lee and Jarvis fail to teach or suggest a test device comprising parallel first and second memory cell structures disposed in a scribe line region, each having a deep trench capacitor and a vertical transistor structure formed in a substrate, as recited in claim 1.

MPEP 2142 reads in part:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

In the office action, the Examiner relies on structures 71 and 73 shown in Fig. 9 and described in paragraph 0085 of Wang to teach the first and second memory cells of claim 1. With reference to paragraph 0056 of the patent, the Examiner states on page 4 of the office action

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that the disclosure made by Wang also encompasses vertical transistors because it is disclosed that the capacitors are stacked and in a trench which are etched in the layers.

Applicant first notes that the structures labeled 71 and 73 shown in Fig. 9 of Wang refer to a *bit line* and a *dummy bit line*, respectively, rather than first and second memory cells as stated by the Examiner in the rejections. See paragraphs 0086 and 0100 of Wang in this regard.

Furthermore, as shown in the figures of the patent, Wang only teaches plane transistors. Thus, even given that the capacitors 36 are tubular capacitors as described in paragraph 0056 of Wang, there is no teaching that the transistors disclosed in Wang are vertical transistors.

Finally, as clearly recited in amended claim 1, the deep trench capacitor and vertical transistor structure is formed *in the substrate*. In contrast, as acknowledged by the Examiner on page 4 of the office action, the capacitors in Wang are etched in the layers.

It is therefore Applicant's belief that even when taken in combination, the prior art references relied upon by the Examiner do not teach or suggest all the limitations of claim 1. For at least this reason, a *prima facie* case of obviousness cannot be established in connection with these claims. Furthermore, as it is Applicant's belief that a *prima facie* case of obviousness is not established for claim 1, the Examiner's arguments in regard to the dependent claims are considered moot and are not addressed here. Allowance of claims 2 and 4-5 is respectfully requested.

There is no motivation to Wang with Lee in the manner described in the office action.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

As described in paragraph 0044 of Wang, the test structure disclosed therein is used for creation of a cross comb bit line design and for detection and identification of diagonal or horizontal bridging between two capacitors in a DRAM structure. Such a method detects

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leakage current to determine if there is a physical bridge between two capacitors, rather than detecting alignment of active areas and memory cell structure by measured resistances. There is no motivation in the prior art to modify Wang's or Lee's disclosure to obtain a test device for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors with the features recited in claim 1.

Foreign Priority Claim

Acknowledgment of receipt of the certified copies of the priority document is respectfully requested. Applicant notes that a certified copy of the priority document was filed on September 29, 2003 with the filing of the application and is shown in the Image File Wrapper on PAIR.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



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